Influence of double-barrier quantum well asymmetry on RTD switching time

Héctor J. De Los Santos and Joel N. Schulman*

Hughes Space and Communications Company, Los Angeles, CA 90009
*Hughes Research Laboratories, Malibu, CA 90265

ABSTRACT

The influence of double-barrier quantum well asymmetry on the switching time of RTDs is studied. For circuit simulation purposes the RTD is modeled as a resistance in series with a parallel combination of a non-linear dependent current source and a non-linear capacitor. The current source embodies an analytic expression for the I(V) characteristics derived from basic principles. The capacitor embodies a C(V) equation derived from a self-consistent numerical two-band model simulation of the structure. It is found that the switching time is most sensitive to asymmetry on the emitter-side barrier, and that the smallest emitter barrier width structure exhibits the smallest switching time.

Keywords: RTD, switching time, high-speed, analytic model, analog, digital, circuit simulation, SPICE, tunneling time.

1. INTRODUCTION

As the level of maturity of RTD fabrication technology advances, a number of possibilities for RTD device structures/materials are being actively pursued for potential application in high-speed analog and digital circuits and systems[1-6]. Since the properties of quantum devices, in general, and RTDs in particular, are highly sensitive to the structural dimensions, it is important to assess the level of control that must be achieved in the growth of a given device structure, in order to fully realize and exploit its high-speed potential. The high-speed properties of quantum devices have been characterized by calculating the *traversal or tunneling time*, i.e., the time a particle takes to traverse the structure. Due to the fact that time in quantum mechanics is regarded not as an observable represented by a Hermitian operator but rather as a parameter or *c*-number, a number of indirect prescriptions have been reported in the literature for the estimation of tunneling time, however, each yielding different result[7]. Furthermore, the calculated times are difficult to related to the device's speed performance in a actual circuit. In this paper we present a study of the influence of double-barrier quantum well asymmetry on RTD switching time by simulating and *observing* the switching action of an RTD embedded in a pulse-forming circuit via SPICE.

2. RTD DEVICE MODEL FOR CIRCUIT SIMULATION

2.1 Analytic RTD current-voltage equation

The RTD circuit model adopted consists of a resistance in series with a parallel combination consisting of a non-linear dependent current source and a non-linear capacitor The non-linear dependent current source embodies an analytic expression for the current-voltage characteristics derived from basic principles[8].

The current-voltage expression contains physical quantities which can also be treated as empirical parameters for increasing levels of physical realism. The genesis of the equation lies on Coon and Liu's[9] model for negative resistance in zero temperature limit. Our approach extends this to include the essential features of non-zero temperature and Fermi-Dirac statistics. We start from the standard formula[10] for the current in the effective mass approximation:

0-8194-2068-9/96/$6.00

$$J = \frac{em^* kT}{2\pi^2\hbar^3}\int_0^\infty dE\,\mathrm{T}(E,V)\ln\left[\frac{1+e^{(E_F-E)/kT}}{1+e^{(E_F-E-eV)/kT}}\right] \tag{1}$$

$$T(E,V) = \frac{(\Gamma/2)^2}{[E-(E_r-eV/2]^2+(\Gamma/2)^2}\ . \tag{2}$$

The transmission coefficient is approximated by a Lorentzian. E is the energy measured up from the emitter conduction band edge. E_Γ is the energy of the resonant level relative to the bottom of the well at its center. G is the resonance width. This formula assumes equal width barriers and that half the voltage drop falls from the emitter to the center of the well. This assumption is not always valid. For better generality eV/2 can be replaced here and in the following equations by eVn with n determined from analysis or fitting.

For small Γ, the transmission coefficient is negligible except when E is close to the resonance, i.e., $E=E_\Gamma-eV/2$. Calculations show that Γ is on the order of one meV or less for even quite thin barrier widths[11]. This is much less than kT at room temperature. Therefore the substitution $E=E_\Gamma-eV/2$ can reasonably be made in the log term and it can be taken outside the integral. The integral is simple and the result is:

$$J = \frac{em^* kT\Gamma}{4\pi^2\hbar^3}\ln\left[\frac{1+e^{(E_F-E_r+eV/2)/kT}}{1+e^{(E_F-E_r-eV/2)/kT}}\right]\left(\frac{\pi}{2}+\tan^{-1}\left(\frac{E_r-eV/2}{\Gamma/2}\right)\right) \tag{3}$$

This formula can be regarded as providing the correct *form* for the lineshape, but calculated in an oversimplified way. The physical quantities can be allowed to depart from their actual values so as to compensate for the approximations and omissions in the model. The following form is the result:

$$J_1(V) = A\ln\left[\frac{1+e^{(B-C+n_1V)e/kT}}{1+e^{(B-C-n_1V)e/kT}}\right]\left(\frac{\pi}{2}+\tan^{-1}\left(\frac{C-n_1V}{D}\right)\right)\ . \tag{4}$$

So far this form produces a peak current and a negative resistance, but there is no increasing valley current, which is due to tunneling through other channels and inelastic scattering. The simplest way to include a valley current contribution is to give it the form of tunneling through a higher resonance or thermal excitation over a barrier. For voltages below this higher energy channel, the additional current takes on the familiar diode form $J_2(V) = H\left(e^{n_2eV/kT}-1\right)$. Second or higher resonances can also be explicitly included if desired, using additional terms similar to J_1.

Figure 1a shows a comparison between measured data and a fit using the sum $J(V)=J_1(V)+J_2(V)$. The RTD is made from $In_{0.53}Ga_{0.47}As/AlAs$ with 26Abarriers and a 48A well. 265A lightly doped spacer layers were sandwiched by highly doped contact layers. The fitting parameters used were $A=10^4$, B=0.035, C=0.1472, D=0.0052, n_1=0.115, $H=1.411\times10^{-1}$, n_2=0.1201.

2.2 RTD capacitance-voltage equation

The non-linear capacitor embodies a capacitance-voltage characteristic derived from a self-consistent numerical two-band model[12] simulation of the structure. To compute the RTD capacitance we proceed as follows: (1) we conceptually partition the device structure into a core section consisting of the barrier/well/barrier (BWB), and an

outer section consisting of the left- and right-hand claddings; (2) The energy profile across the BWB is modified to reflect a linear voltage drop across this part of the structure; (3) The charge distribution corresponding to the applied potential profile across the BWB is obtained quantum mechanically by solving Schrödinger's equation over the energies of all electrons impinging onto the BWB from the emitter-side, using a transfer matrix technique; (4) The electric field within the BWB is computed by solving Poisson's equation; (5) The electric field at the barrier/cladding interfaces together with the assumption of zero electric field at the contacts, are used as boundary conditions to solve Poisson's equation following Kireev's approach[13] in the cladding region and obtain the band bending.; (6) The procedure (1)-(5) is repeated until the potential profile in the BWB doesn't change (to within a given tolerance); (7) The capacitance is obtained by calculating $C = \frac{\partial Qcladding}{\partial V}$, where $Q_{cladding} = E_{barrier/cladding\ interface}\varepsilon\varepsilon_0/q$, where ε and ε_0 is the relative permittivity and permittivity, respectively, and q is the electron charge. The functional form

$$C_{RTD} = \frac{C_{jo}}{\left(1+\frac{|V|}{V_{bi}}\right)^{M}} \tag{5}$$

which fits the calculated curve C(V), Figure 1b, is used. This curve was calculated for a $7\mu m^2$ InAs/AlAs RTD, to be described in next section, with BWB widths of 9.5/16/9.5 monolayers. The parameters are Cjo=0.0261pF, V_{bi}=0.1875, and M=0.1774.

3. ASYMMETRY DEPENDENCE OF RTD SWITCHING TIME

To assess the influence of structural asymmetry on RTD switching time we have simulated in SPICE3f5 a pulse-forming circuit[14]. This circuit, which is similar to that used for performing electro-optic sampling measurements, was utilized because while simulating the device in a circuit environment, it allows for its intrinsic device time response to be clearly observed. It consists of a 50Ω ideal transmission line with an RTD shunted to ground. The input voltage source creates a voltage step which propagates down the transmission line. When the step reaches the diode, the resulting waveform of its turn on switching transient is clearly displayed for various RTD barrier layer thicknesses. The observed 10-90% switching transition time is taken as a measure of the device switching speed. To conduct the study we have chosen to simulate an InAs/AlAs RTD with collector-barrier/well/emitter-barrier widths of 9.5/16/9.5 monolayers (ML). The cladding was assumed to be 250 Angstroms, and to be n-doped to $10^{17}cm^{-3}$. Five COLLECTOR/EMITTER barrier asymmetries were considered, namely, 5.5/9.5, 7.5/9.5, 9.5/9.5, 9.5/7.5, 9.5/5.5, where the first number refers to the number of monolayers making up the collector-side barrier, and the second refers to that making up the emitter-side barrier.

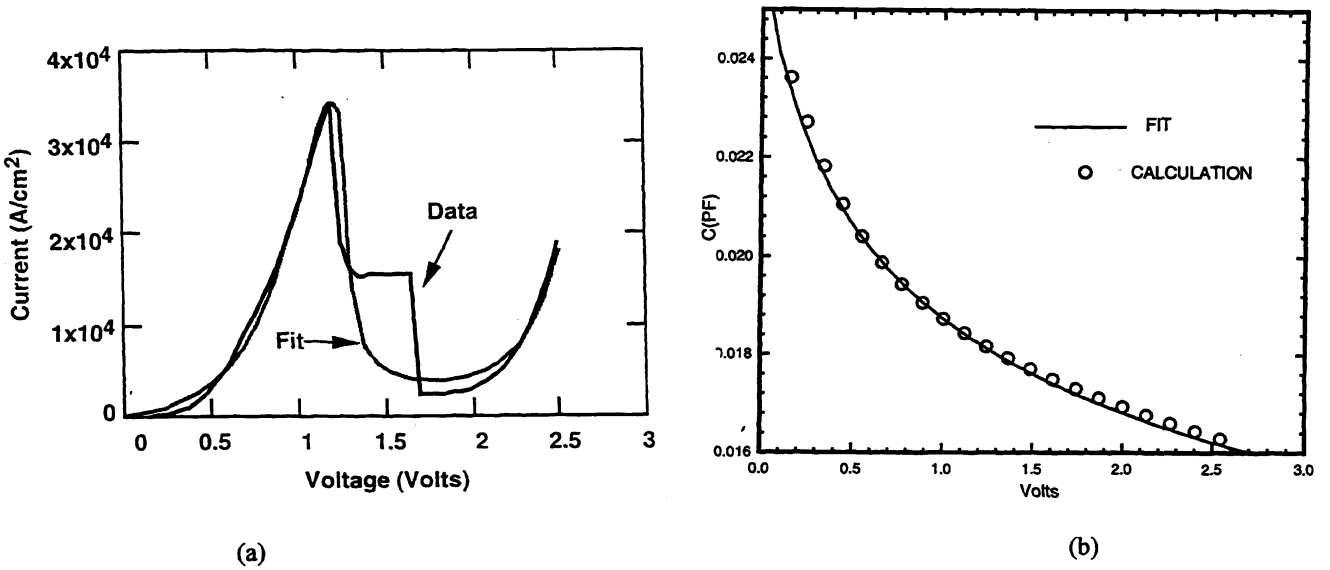
Figures 2 through 4 show the calculated Current-Voltage, Capacitance-Voltage, and Voltage switching transient curves for RTDs with various degrees of asymmetry. As can be seen in Fig. 2, asymmetries on the collector-side barrier have considerably less effect on the peak current than asymmetries on the emitter-side barrier. In fact, while a 42% decrease in the collector barrier width induces a 25% increase in the peak current, the same percentual decrease on the emitter barrier width causes a 552% increase in the peak current. On the other hand, a determination of the switching time, see Table 1, reveals that the 9.5/5.5 structure maintains the smallest switching time, at 0.83psec, followed by the symmetric 9.5/9.5 case at 0.91psec, and then the 5.5/9.5 case at 0.96psec. This trend on switching time behavior is related to the effect of the asymmetry, not just on the peak current, but also the valley voltage and thus the voltage swing the device charges to. In particular, we see in Figure 3a that while the collector-side asymmetry induces a lower peak current than the emitter-side one, it is accompanied by a lower valley voltage. Structure asymmetry has virtually no effect on the device capacitance, see Figure 3b; a result of the fact that , despite the asymmetry, the total device length remained constant. Considering now Figure 4 in light of Figure 2, the following conclusion can be drawn: (1) asymmetries on the collector-side barrier induce changes only on the peak current, whereas those on the emitter-side barrier induce large changes on *both* the peak voltage and the valley

voltage. This seems to be responsible for the behavior shown in Figure 4, namely, the switching time is virtually insensitive to an asymmetry on the collector-side barrier, Figure 4a, while its rather sensitive to an asymmetry on the emitter-side barrier, Figure 4b. A look at the internal electron charge distribution reveals that reducing the emitter barrier strongly increases the electron supply into the well, thus increases the peak current, and therefore, reduces the switching time.

In conclusion, we have studied the effect of asymmetry on RTD switching time by constructing a circuit model for the device, embedding it into a pulse-forming circuit, and performing simulations in SPICE3f5 for various degrees of barrier asymmetry. We have found that the RTD switching time is extremely sensitive to variations on the emitter-side barrier width, and that this sensitivity is related to the induction of dramatic changes on both the peak current and the valley voltage, and on the number of electrons tunneling through the emitter barrier. Our simulation results suggest that, for fast switching applications, the emitter barrier width may be used to tailor the switching time.

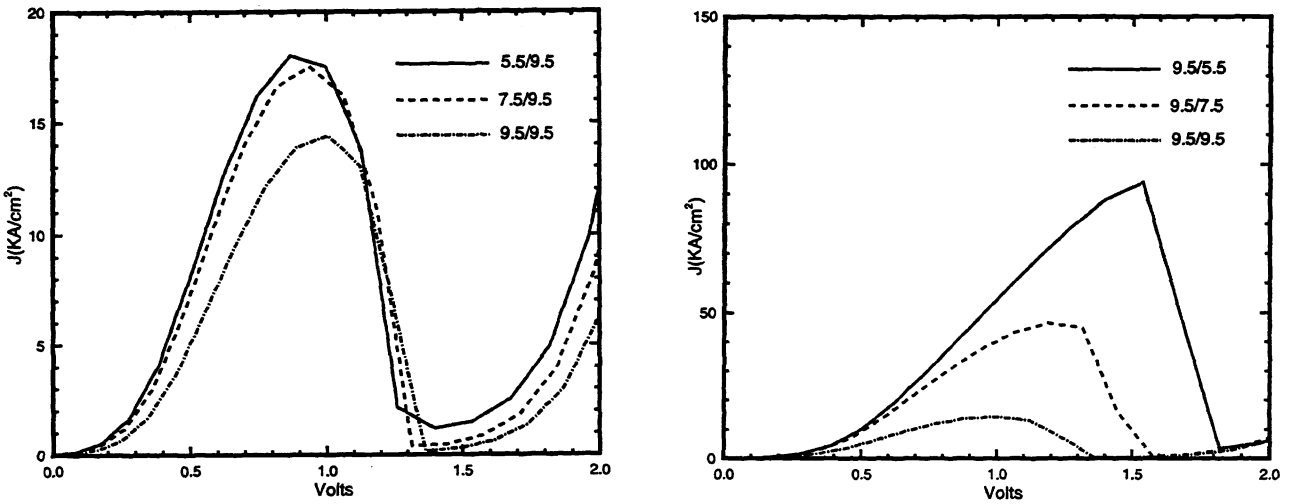
4. REFERENCES

1 F. Capasso, S. Sen, A.Y. Cho, and D. Sivco, *IEEE Electron Device Lett.*, vol. EDL-8, pp. 297-299, 1987.
2 S.J. Wei, H.C. Lin, R.C. Potter, and D. Shupe, *IEEE J. Solid-State Circuits*, vol. 28., no. 6, pp.697-700, 1993.
3 A.C. Seabaugh, et al., *Electronic Letts.*, vol. 29, no. 20, pp.1802-1803, 1993.
4 C.E. Chang, P.M. Asbeck, K.C. Wang, and E.R. Brown, *IEEE Trans. Electron Devices*, vol. 40, pp.685-691, 1993.
5 Z.X. Yan and M. J. Deen, *IEEE J. Solid-State Circuits*, vol. 27, no. 8, pp. 1198-1202, 1992.
6 J. Shen, G. Kramer, S. Tehrani, H. Goronkin and R Tsui, *IEEE Electron Device Lett.*, vol. 16, no. 5, pp.178-180, 1995.
7 A.F.M. Anwar and M.M. Jahan, *IEEE J. Quan. Electron.*, vol. 31, No. 1, pp. 3-7, 1995.
8 J.N. Schulman and H.J. De Los Santos, *Proc. Int. Sem. Dev. Res. Symp.*, Dec. 5-8, 1995, Charlottesville, VA.
9 D.D. Coon and H.C. Liu, "Frequency limit of double barrier resonant tunneling oscillators," *Appl. Phys. Lett.* **49**, (1986), pp. 94-96.
10 R. Tsu and L. Esaki, "Tunneling in a finite superlattice," *Appl. Phys. Lett.* **22**, (1973), pp. 562-564.
11. D. H. Chow, J. N. Schulman, E. Ozbay, and D. M. Bloom, "1.7-ps microwave integrated circuit-compatible InAs/AlSb resonant tunneling diodes," Appl. Phys. Lett. 61, (1992), pp. 1685-1687.
12 J.N. Schulman, "$Ga_{1-x}Al_xAs$-$Ga_{1-y}Al_yAs$-GaAs double-barrier structures," *J. of Appl. Phys.* **60**, (1986), pp. 3954-3958; J.N. Schulman and M. Waldner, "Analysis of second level resonant tunneling diodes and transistors," *J. of Appl. Phys.* **63**, (1988), pp. 2859-2861.
13. P.S. Kireev, *Semiconductor Physics,* Chapter VI, MIR Publishers, Moscow, 1978.
14 E. Ozbay, D.M. Bloom, D.H. Chow, and J.N. Schulman, IEEE Elec. Dev. Lett., vol. 14, No. 8, pp. 400-402, 1993.



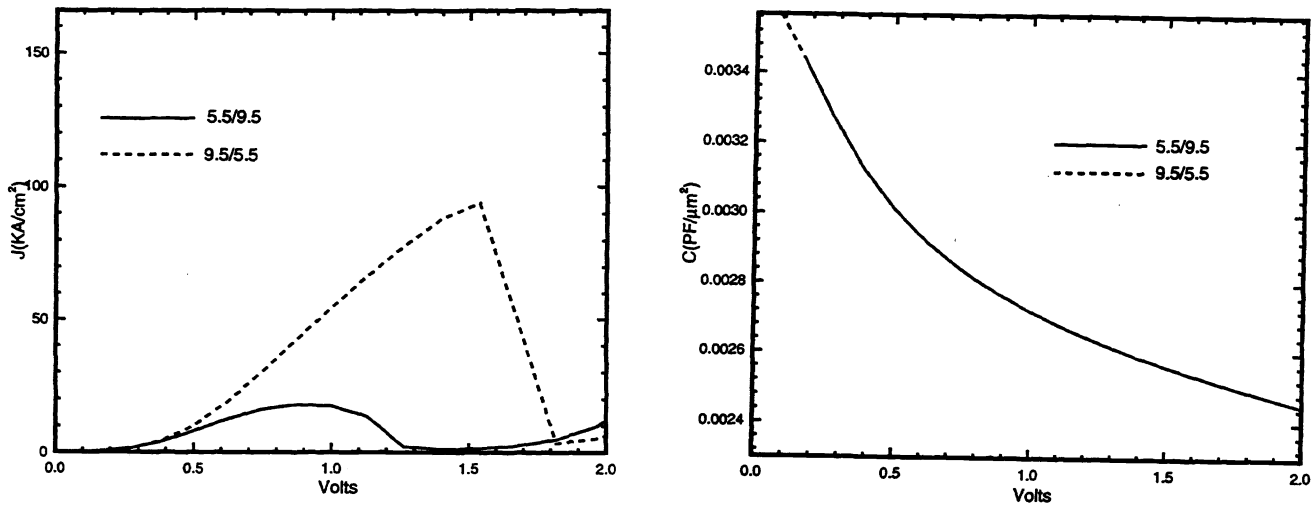
(a) (b)

Figure 1. (a) Comparison of measured InGaAs/AlAs RTD I(V) and model fit. (b) Comparison of calculated InAs/AlAs RTD C(V) and equation fit.



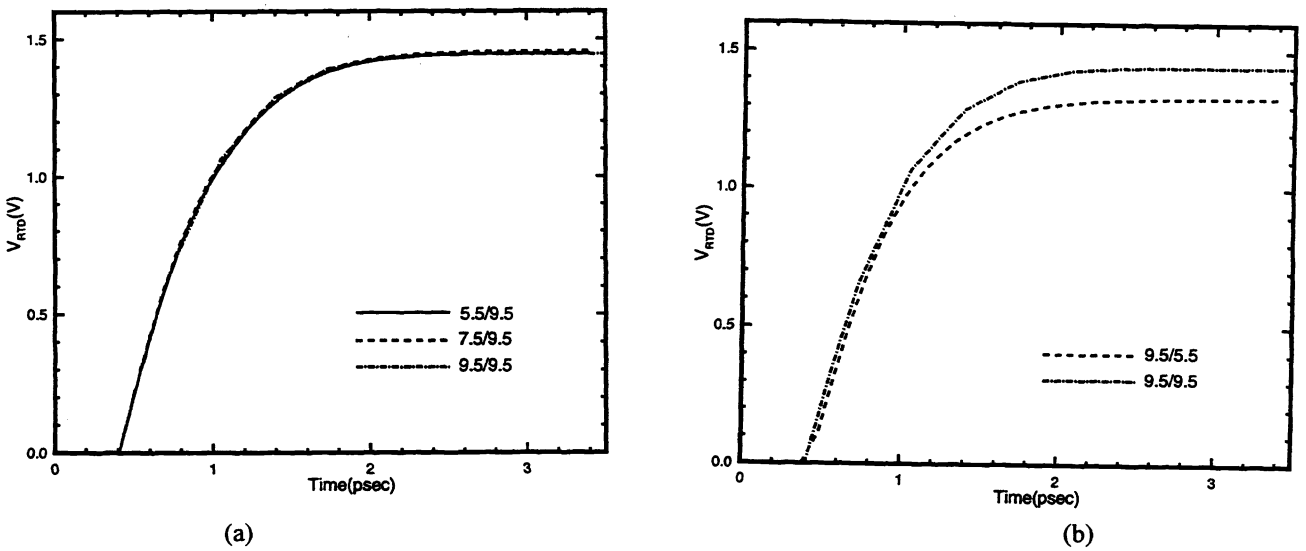
(a) (b)

Figure 2. Calculated InAs/AlAs RTD I(V) characteristic for: (a) varying collector/constant emitter barrier width,and (b) constant collector/varying emitter barrier width (in monolayers).



(a) (b)

Figure 3. Comparison of calculated InAs/AlAs RTD characteristics for extreme collector/emitter barrier width asymmetries: (a) I(V), (b) C(V).



(a) (b)

Figure 4. Calculated InAs/AlAs RTD voltage switching transients for: (a) varying collector/constant emitter barriers widths, (b) constant collector/varying emitter barrier widths (in monolayers).

Table 1. Calculated Peak Current and Switching Time of InAs/AlAs RTD for various barrier asymmetries.

COLLECTOR/EMITTER BARRIER WIDTH (ML)	PEAK CURRENT (kA/cm^2)	SWITCHING TIME (10-90%) (psec)
5.5/9.5	18	0.96
7.5/9.5	17	-
9.5/9.5	14	0.91
9.5/7.5	46	-
9.5/5.5	93	0.83